

**Amendments to the Specification:**

Please replace the section added in the Amendment filed August 26, 2004 beginning at page 11, between lines 17 and 18, with the following redlined section:

**BRIEF SUMMARY OF THE INVENTION**

The invention relates to an area-efficient realization of a coefficient block with hardware sharing techniques and optimizations applied to this block. The block is connected to coefficient lines coming from a delay block to be connected to perform a filtering operation or a mathematical computing operation with optimization in hardware and provides a zero latency output. The invention also gives the area minimal realization of digital filters based on the coefficient block, when operated in serial bit fashion. The optimization techniques and structure of the present invention are good for bit-serial digital filters typically a finite impulse response (FIR) filter, including finite impulse response filter (IIR) and for other filters and applications based on combinational logic that includes delay elements, multipliers, and serial adders and/or subtractors.

**BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS**

~~Figure 1 shows~~Figures 1A-1C show the field of the invention and applications of the device.

~~Figure 2 shows~~Figures 2A-2G show the symbol of components used in the device.

~~Figure 3 shows~~Figures 3A-3D show the description of components used in the device.

~~Figure 4 shows~~Figures 4A-4B show bit-serial FIR filter implementations.

Figure 5 shows an example of a FIR filter.

Figure 6 shows one of the known minimization technique due to symmetry of coefficients.

Figure 7 shows the structure of a prior/known implementation technique for a coefficient block.

Figure 8 shows the generalized structure of a prior/known implementation technique for a coefficient block.

Figure 9 shows the minimization technique involved in a FIR filter.

Figure 10 shows the generalized structure of the minimization technique involved in the FIR filter.

Figure 11 shows the minimized structure of this example FIR filter, of the present invention.

~~Figure 12 shows~~ Figures 12A-12B show the generalized optimized structure of the present invention.

Figure 13 shows the other advantage of the structure, i.e., getting the parallel output directly, of the present invention.